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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,968	03/26/2004	Joseph S. Cavallo	P18330	7920

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EXAMINER	
KAWSAR, ABDULLAH AL	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,968	CAVALLO, JOSEPH S.	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 are pending.

Specification

2. The abstract of the disclosure is objected to because the abstract is too short and fails to provide a proper disclosure of the invention. Correction is required. See MPEP § 608.01(b).

3. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claims languages are not clearly understood:

i. As per claim 1, line 2 recites "permitting a thread" is not clear what constitutes permitting a thread to be interrupted (i.e. thread has interrupt enable/ disable function? some type of flag or value that allows the thread to be interrupted?). Line 4 recites "selectively setting the thread to restart" it is unclear what constitutes selectively setting the thread to restart (i.e. some value/flag/ indicator defines which one to restart or not..? what is criteria for selecting?).

ii. Claims 9, 18, 21, 29 and 37 has similar deficiency as of claim 1 above.

iii. Claim 9, line 3 recites "selectively incrementing a count number" it is unclear what constitutes selectively incrementing a count number (i.e. what is the criteria for selectively incrementing). Line 6 recites "selectively saving program stack condition" it is unclear what constitutes selectively saving the program stack condition.

iv. Claim 18 has similar deficiency as of claim 9 above.

v. Claim 16, line 2 recites "selectively disabling interrupts" it is unclear what constitutes selectively disabling interrupts in critical region (i.e. what is the criteria for selecting the interrupts to be disabled?).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 7-8, 18-19, 21-22, 27-30 and 35-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Dice et al. US Patent Publication No. 2004/0025160.

8. As per claim 1, Dice teaches the invention as claimed including a method comprising:

permitting a thread to be interrupted during a first critical region (par. 0041);

interrupting the thread with an interrupt routine (par. 0042); and

selectively setting the thread to restart at a beginning of the first critical region in response to an indication that the thread is working in a critical region (par. 0017).

9. As per claim 2, Dice teaches wherein the setting the thread to start at the beginning of the first critical region comprises: setting a stack pointer and program counter so that the interrupted thread restarts at the beginning of the first critical region (par. 0049; par. 0050; par. 0051).

10. As per claim 7, Dice teaches marking the thread as having been interrupted during the first critical region (par. 0041).

11. As per claim 8, Dice teaches indicating that the thread is not operating in a critical region (par. 0057; clearing the "INCRIT" bit if thread is not in critical region operation).

12. As per claim 18, Dice teaches the invention as claimed including a method comprising:

permitting a critical region to be interrupted (par. 0041); and

selectively saving stack conditions of an interrupted critical region in response to the critical region not having been previously interrupted (par. 0041 and 0042).

13. As per claim 19, Dice teaches commencing work in the critical region (par. 0041, lines 1-3).

14. As per claim 21-22, 27-28, they have similar limitations as of claims 1-2 and 7-8 above. Therefore they are rejected under the same rational as of claims 1-2 and 7-8 above.

15. As per claim 29-30 and 35-36, they have similar limitations as of claims 1-2 and 7-8 above. Therefore they are rejected under the same rational as of claims 1-2 and 7-8 above.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3-6, 9-17, 20, 23-26, 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dice et al. US Patent Publication No. 2004/0025160, in view of Benson et al. US Patent No. 5542076.

18. As per claim 3, Dice do not specifically disclose wherein the first critical region includes the acts of: selectively incrementing a count of a number of times the first critical region has been interrupted in response to the first critical region having been previously interrupted (col 7, lines 12-35); and selectively saving program stack conditions of the interrupted thread in response to the thread not having been interrupted during the first critical region more than a maximum permitted number of times.

However wherein the first critical region includes the acts of: selectively incrementing a count of a number of times the first critical region has been interrupted in response to the first critical region having been previously interrupted (col 5, lines 12-35); and

selectively saving program stack conditions of the interrupted thread in response to the thread not having been interrupted during the first critical region more than a maximum permitted number of times (col 5, lines 12-35; lines 57-67 through col 6, lines 1-4).

19. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Benson into the method of Dice to incrementing a number of times the critical region has been interrupted and saving the program stack conditions of the interrupted thread in response the thread not being interrupted more then a maximum permitted number. The modification would have been obvious because one of the ordinary skills

of the art would utilize the teaching of Benson to disable the interrupt service if the critical region has been interrupted more than a permitted number of times to be able to finish the system operation without taking a long time and create uncertainty within the thread operations.

20. As per claim 4, Dice teaches wherein the first critical region further includes the acts of: setting a flag to indicate that a critical region is entered (par. 0041, lines 1-6);

performing critical region interrupt recovery work in response to an indication that the first critical region was previously interrupted (claim 1, D, lines 1-4); and

attempting to complete first critical region work (par. 0051).

21. As per claim 5, Dice teaches wherein the critical region interrupt recovery work corrects errors that arise from previously interrupting the first critical region prior to its completion (par. 0018, lines 6-21).

22. As per claim 6, Dice teaches wherein the first critical region further includes the acts of: selectively setting a flag to indicate that critical region work is not being performed in response to the critical region work completing (par. 0057); and

Dice do not specifically disclose setting to zero the count of the number of times the first critical region was interrupted.

However Benson teaches setting to zero the count of the number of times the processing was interrupted (col 7, lines 17-20).

23. As per claim 9, Dice teaches the invention substantially as claimed including a method comprising:

permitting a thread to be interrupted during a first critical region (par. 0041);

selectively saving program stack conditions of the interrupted thread in response to the thread having been interrupted during the first critical region (par. 0049; par. 0050; par. 0051).

Dice do not specifically disclose selectively incrementing a count of a number of times the first critical region has been interrupted in response to the first critical region having been previously interrupted; and thread not having been interrupted during the first critical region more than a maximum permitted number of times.

However Benson teaches selectively incrementing a count of a number of times the processing task has been interrupted in response to the processing having been previously interrupted(col 5, lines 12-35); and

thread not having been interrupted during the processing more than a maximum permitted number of times(col 5, lines 12-35; lines 57-67 through col 6, lines 1-4).

24. As per claim 10-11 and 13, they have similar limitations as of claims 4-5 and 6 above. Therefore they are rejected under the same rational as of claims 4-5 and 6 above.

25. As per claim 12, Dice teaches commencing work in the first critical region (par. 0041, lines 1-3).

26. As per claim 14, Dice teaches setting a flag to indicate that a critical region is entered (par. 0041, lines 1-6); and

selectively commencing work in the first critical region in response to an indication that the first critical region was not previously interrupted (par. 0049; par. 0050).

27. As per claim 15, it has similar limitations as of claim 6 above. Therefore it is rejected under the same rational as of claim 6 above.

28. As per claim 16, Dice teaches the invention substantially as claimed including a method comprising:

critical region having been interrupted (par. 0041); and

commencing critical region work (par. 0041, lines 1-3).

Dice do not specifically disclose selectively disabling interrupts in response to the critical region having been interrupted more than a permitted number of times.

However Benson teaches selectively disabling interrupts in response to the processing having been interrupted more than a permitted number of times (col 2, lines 26-32; col 5, lines 57-67 through col 6, lines 1-4);

29. As per claim 17, Dice teaches selectively setting a flag to indicate that critical region work is not being performed in response to the critical region work completing(par. 0057);

Dice do not specifically disclose selectively resetting a counter of times the critical region was interrupted to zero in response to the critical region work completing; and re-enabling interrupts of the critical region.

However Benson teaches resetting a counter of times the task processing was interrupted to zero in response to the task processing work completing (col 5, lines 23-35; col 7, lines 17-20); and

re-enabling interrupts of the task processing (col 5, lines 23-35).

30. As per claim 20, it has similar limitations as of claim 6 above. Therefore it is rejected under the same rational as of claim 6 above.

31. As per claim 23-26, they have similar limitations as of claims 3-6 above. Therefore they are rejected under the same rational as of claims 3-6 above.

32. As per claim 31-34, they have similar limitations as of claims 3-6 above. Therefore they are rejected under the same rational as of claims 3-6 above.

33. Claims 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dice et al. US Patent Publication No. 2004/0025160, in view of Nelson et al. US Patent No. 6446141.

34. As per claim 37, Dice teaches the invention substantially as claimed including a system comprising:

a first storage subsystem and a second storage subsystem (par. 0031, lines 1-5);

a first circuit card including first circuitry capable of being coupled to the first storage subsystem, wherein the first circuitry further includes an I/O controller device, the I/O controller device comprising: a processor; a memory device, wherein the memory device includes code segments that instruct the processor to (par. 0031 and par. 0032):

permit a thread to be interrupted during a first critical region, interrupt the thread with an interrupt routine, and selectively set the thread to restart at a beginning of the first critical region in response to an indication that the thread operates in a critical region(par. 0041; par. 0042; par. 0017); and

Dice do not specifically disclose a second storage subsystem and a second circuit card including second circuitry capable of being coupled to the second storage subsystem.

However Nolan teaches a second storage subsystem (col 13, lines 33-35); and

a second circuit card including second circuitry capable of being coupled to the second storage subsystem (col 13, lines 33-35; col 5, lines 3-7; col 6, lines 29-35).

35. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Nolan into the method of Dice to have a second storage system connected to a second circuit card. The modification would have been obvious because one of the ordinary skills of the art would utilize the teaching of Nolan to have multiple different circuitry as I/O controller for supporting different storage system to increase the system efficiency.

36. As per claim 38, Nolan teaches wherein the second circuit includes an I/O controller device (col 3, lines 40-41; col 13, lines 33-35; SCSI controller).

37. As per claim 39, Nolan teaches wherein the first storage subsystem and the second storage subsystem each comprise one or more respective mass storage devices (col 2, lines 51-54).

38. As per claim 40, Nolan teaches the first storage subsystem comprises a redundant array of inexpensive disks (RAID) (col 11, lines 52-56); and

the second storage subsystem comprises a tape mass storage system (col 13, lines 33-35).

39. As per claim 41, Nolan teaches a circuit board coupled to the bus, wherein the circuit board comprising a bus, memory, and a host processor (col 1, lines 55-61; figure 3); and

the first circuit card and the second circuit card are capable of being coupled to the bus (figure 3; col 13, lines 21-35; col 15, lines 25-33).

40. As per claim 42, Nolan teaches wherein the bus complies with PCI (col 2, lines 46-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is

(571)270-3169. The examiner can normally be reached on Monday to Thursday between 8:00am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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